Description

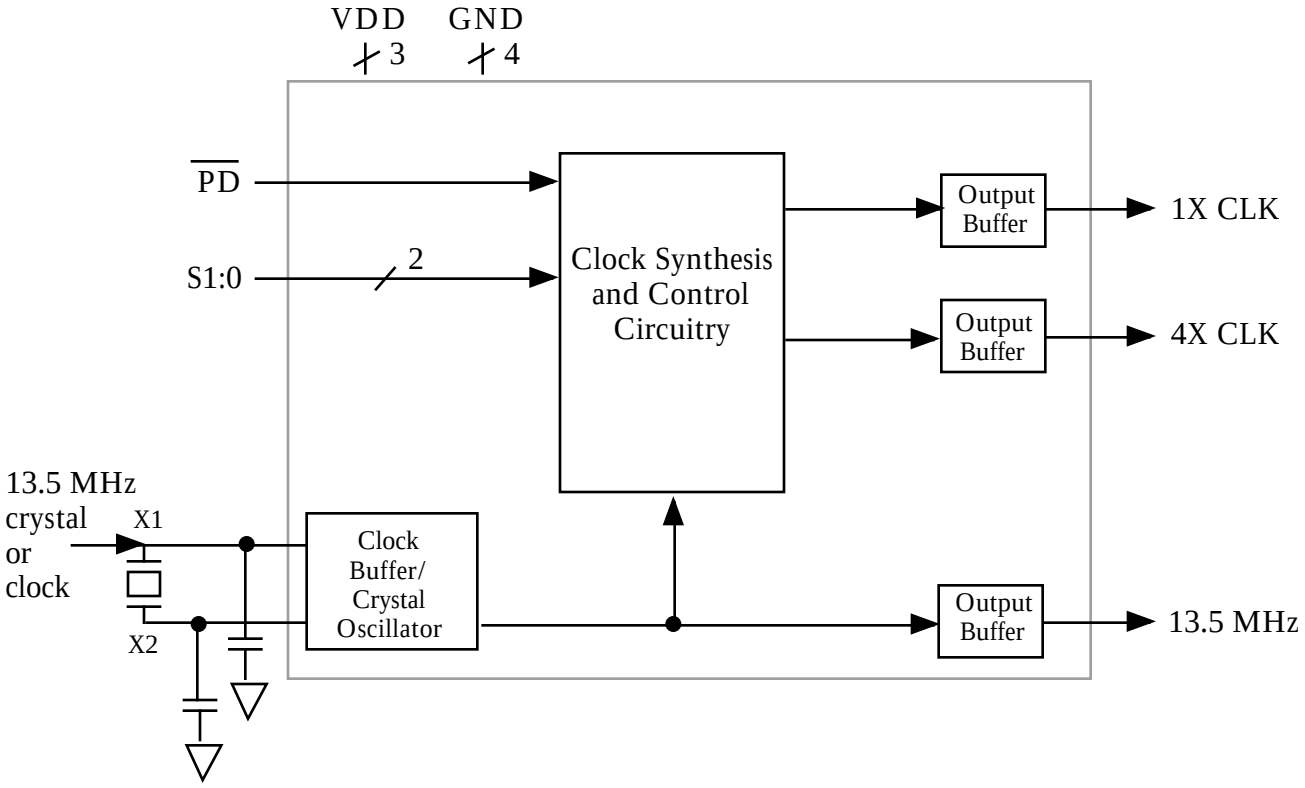
The MK2715 provides clocks for audio systems using NTSC or PAL encoders and decoders. The chip uses MicroClock's proprietary analog Phase-Locked Loop technology, and generates all of the outputs from a 13.5 MHz input crystal or clock. This chip can save component cost, component count, board stuffing cost, and increase reliability by removing mechanical quartz devices from the system.

MicroClock offers many other clocks for audio and video systems. Consult MicroClock when you need to remove crystals and oscillators from your board.

Features

- Packaged in 16 pin narrow (150 mil) SOIC
- Selectable NTSC, PAL, PAL(M), and PAL COMBO N frequencies
- 1X and 4X clock outputs
- Zero ppm error on NTSC and PAL clocks
- Power Down turns off chip, reduces power to microWatt levels
- 5V ±10% supply voltage

Block Diagram



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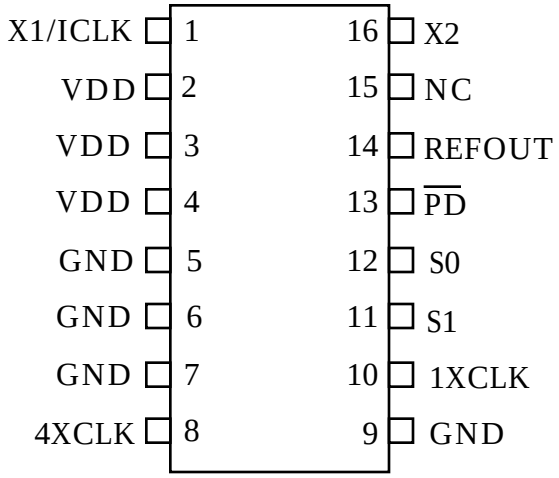
Pin Assignment



16 pin narrow (150 mil) SOIC

Video Clock Select Table (MHz)

S1 pin 11	S0 pin 12	1XCLK pin 10	4XCLK pin 8	Video Standard
0	0	3.5821	14.3284	PAL N
0	1	3.5756	14.3024	PAL M
1	0	4.4336	17.7345	PAL
1	1	3.5795	14.31818	NTSC

Pin Descriptions

Number	Name	Type	Description
1	X1/ICLK	I	Crystal connection. Connect to 13.5000 MHz crystal, or clock input
2	VDD	P	Connect to +5V.
3	VDD	P	Connect to +5V.
4	VDD	P	Connect to +5V.
5	GND	P	Connect to ground.
6	GND	P	Connect to ground.
7	GND	P	Connect to ground.
8	4XCLK	O	4X NTSC/PAL clock output. Determined by S0, S1 per Table above.
9	GND	P	Connect to ground.
10	1XCLK	O	1X NTSC/PAL clock output. Determined by S0, S1 per Table above.
11	S1	I	Clock Select 1. Determines 1XCLK and 4XCLK outputs per Table above.
12	S0	I	Clock Select 0. Determines 1XCLK and 4XCLK outputs per Table above.
13	$\overline{PD}$	I	Power Down. Active low. All clocks stop low and all circuitry is off.
14	REFOUT	O	Buffered 13.5000 MHz clock output.
15	NC	-	No Connect.
16	X2	O	Crystal connection. Leave unconnected for clock input, or connect to 13.5000 MHz crystal.

Type: I = Input, O = output, P = power supply connection

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Electrical Specifications (at 5.0V unless otherwise noted)

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (Note 1)					
Supply Voltage, VDD	Referenced to GND			7	V
Inputs and Clock Outputs		-0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	°C
Soldering Temperature	Max of 10 seconds			250	°C
Storage Temperature		-65		150	°C
DC CHARACTERISTICS					
Operating Voltage, VDD		4.5	5	5.5	V
Input High Voltage, VIH		2			V
Input Low Voltage, VIL				0.8	V
Output High Voltage	IOH=-4mA	VDD-0.4			V
Output High Voltage	IOH=-25mA	2.4			V
Output Low Voltage	IOL=25mA			0.4	V
Operating Supply Current, IDD	No Load		22		mA
Standby Supply Current, IDDPD	No Load, $\overline{PD}$=0V		20		µA
Short Circuit Current	Each output		±100		mA
Input Capacitance	S0, S1 pins		7		pF
Actual mean frequency error versus target, note 2	Ex 14.328, 3.582 MHz			0	ppm
Actual mean frequency error versus target	14.328, 3.582 MHz			14	ppm
AC CHARACTERISTICS					
Input Frequency			13.5		MHz
Output Clock Rise Time	0.8 to 2.0V			1.5	ns
Output Clock Fall Time	2.0 to 0.8V			1.5	ns
Output Clock Duty Cycle	Time above 1.4V	45	49 to 51	55	%
Power down Time, $\overline{PD}$ taken low to clocks off				1	µs
Power up Time, $\overline{PD}$ taken high to clocks stable				10	ms

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.
2. Provided the crystal is properly tuned, or an accurate 13.5000 MHz input clock is used.

External Components/Crystal Selection

The MK2715 requires a minimum number of external components for proper operation. For a crystal input, a parallel resonant 13.5000 MHz crystal is recommended, with frequency tolerance of 50ppm or better. Crystal capacitors should be connected from each of the pins X1 and X2 to Ground. The value (in pF) of these crystal caps should be = $(C_L-8)*2$, where C_L is the crystal load capacitance in pF. For a clock input, connect to X1 and leave X2 unconnected. Multiple VDD and GND pins should be connected together, and a decoupling capacitor of 0.1µF must be connected between them very close to the chip. A 33Ω terminating resistors can be used on clock outputs with traces longer than 1 inch.

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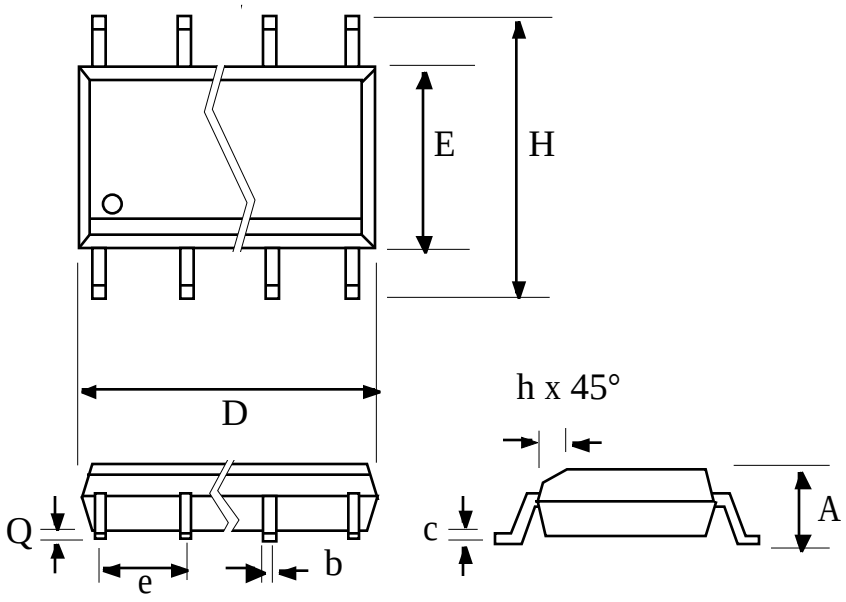
Package Outline and Package Dimensions

16 pin SOIC narrow



	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	0.055	0.070	1.397	1.778
b	0.013	0.019	0.330	0.483
c	0.007	0.010	0.190	0.254
D	0.385	0.400	9.779	10.160
E	0.150	0.160	3.810	4.064
H	0.225	0.245	5.715	6.223
e	.050 BSC		1.27 BSC	
h		0.016		0.406
Q	0.004	0.01	0.102	0.254

Ordering Information

Part/Order Number	Marking	Package	Temperature
MK2715-01S	MK2715-01S	16 pin narrow SOIC	0-70°C
MK2715-01STR	MK2715-01S	Add Tape & Reel	0-70°C

CHANGE HISTORY

Version	Date first published	Comments
A	3/19/97	Original
B	8/15/97	Changed load capacitance equation on page 3.

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